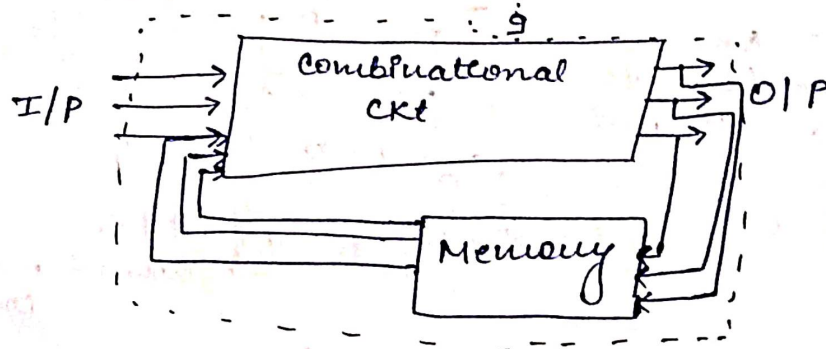
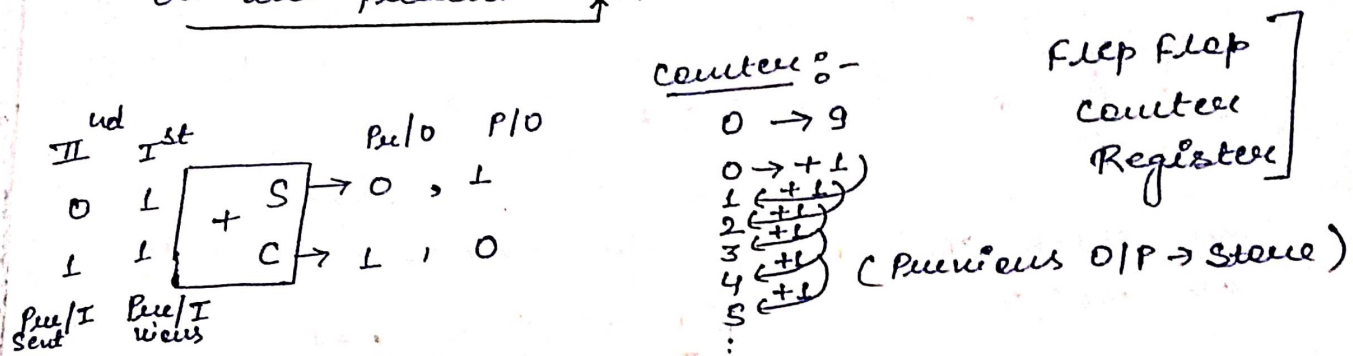


Introduction To Sequential Circuits

- These are the combinational circuits with memory
- In Sequential circuits, the Present O/P depends on the Present I/P as well as Previous O/P.

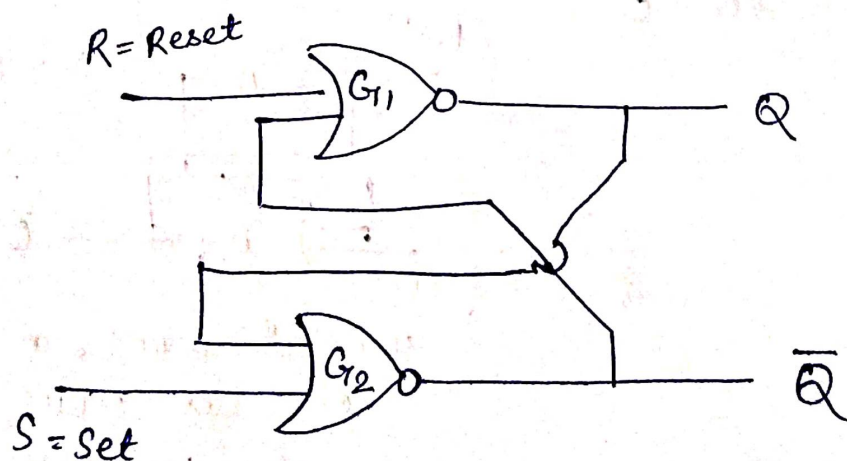


Sequential circuit

0, 1 → store in memory.
Only store 1 bit either 0 or 1
→ Flip Flop
→ Latch

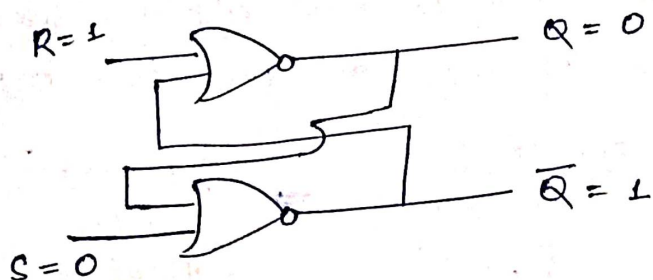
SR LATCH USING NOR Gate :-

→ The basic storage Element is called LATCH.



Reset = $Q = 0, R = 1$
Set = $Q = 1, S = 1$

Case - I
 $S = 0$ $Q = 0$
 $R = 1$ $\bar{Q} = 1$

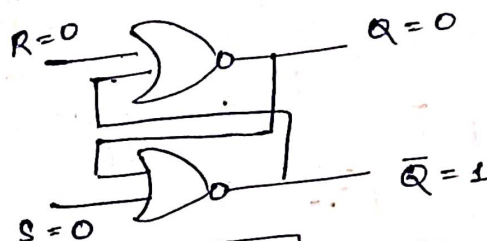


NOR Gate :-

A	B	$Y = \overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

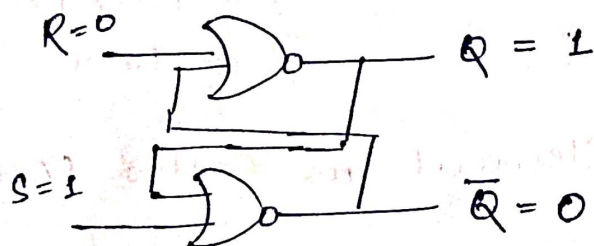
we check this process in store in memory
in net?

$S = 0$ } Remove
 $R = 0$ } both the
 input



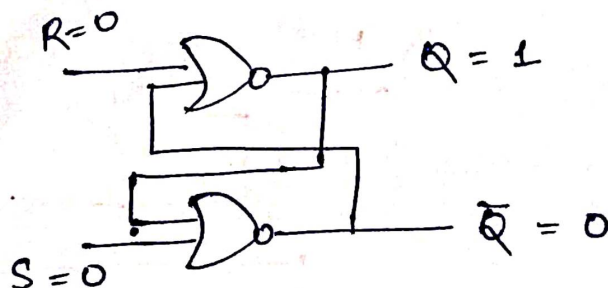
$S = 0, R = 0, Q = 0, \bar{Q} = 1$ → 1 bit stored in the latch.

Case - IInd :- $S = 1$ $Q = 1$ $\bar{Q} = 0$
 $R = 0$



when both the input
are 0

→ $S = 0, Q = 1$
 $R = 0, \bar{Q} = 0$

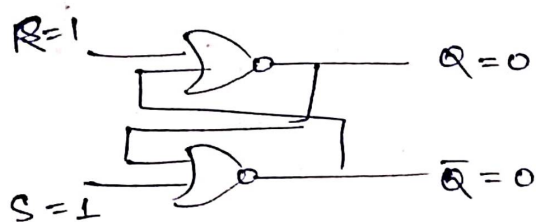


this is work as memory
one bit store
in memory.

Case - IIIrd

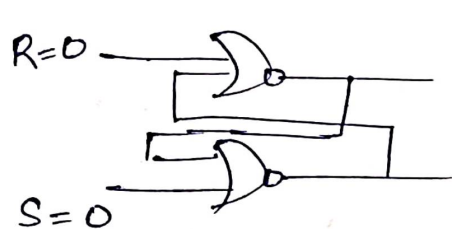
$$S = 1, R = 1, Q = 0, \bar{Q} = 0$$

3.



NOT True
Becoz both are
complementary.

$$S = 0, Q = \\ R = 0, \bar{Q} =$$



$$Q = 0 \text{ 1st, II}^{\text{nd}} \\ \bar{Q} = 0 \text{ 1st, II}^{\text{nd}}$$

$$S = 0 \\ R = 0$$

$$Q = 0, \bar{Q} = 1 \\ Q = 1, \bar{Q} = 0$$

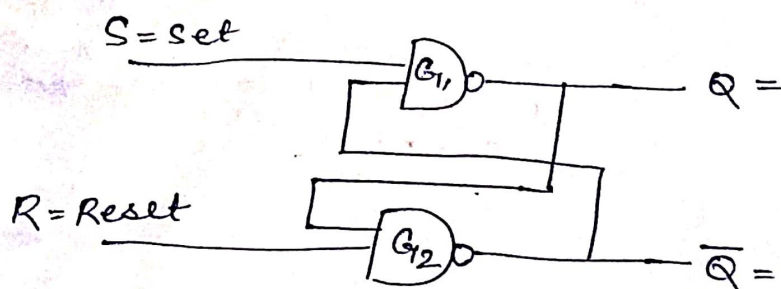
This is contradictory state, in this
 $S = 1, R = 1$ never used.

Truth Table For SR Latch :-

S	R	Q	$\bar{Q}$
0	0	previous state (memory)	
0	1	0	1 Reset
1	0	1	0 Set
1	1	Not used.	

SR LATCH USING NAND GATE :-

4-



Truth Table of NAND

A	B	$Y = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

Set = $Q = 1$
Reset = $Q = 0$

Case-1st

$S = 0$ $Q = 1$
 $R = 0$ $\bar{Q} = 1$ } NOT True

NOT USED THIS STATE

Case-2nd

$S = 1$ $Q = 0$
 $R = 0$ $\bar{Q} = 1$

$S = 1, R = 1$ Previous state state

Case-3rd

$S = 0$ $Q = 1$
 $R = 1$ $\bar{Q} = 0$

$S = 1$ Previous state state
 $R = 1$

Case-4th

$S = 1$ $Q =$
 $R = 1$ $\bar{Q} =$ Previous state

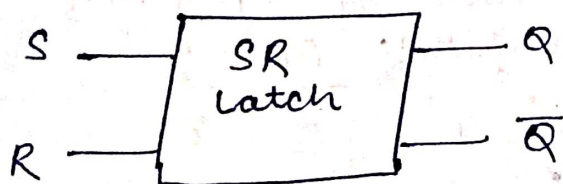
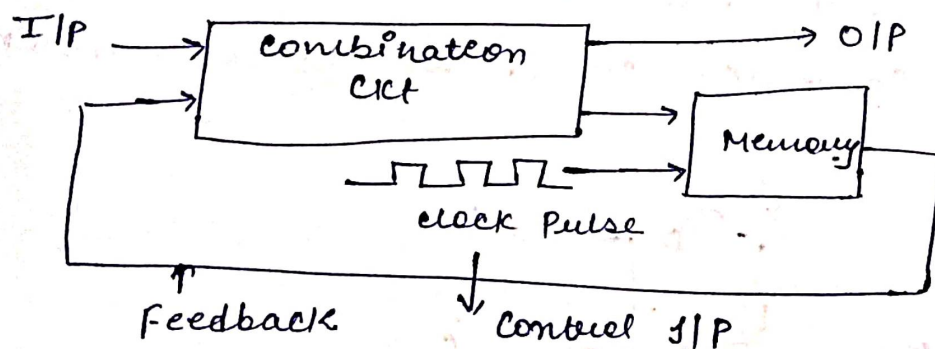
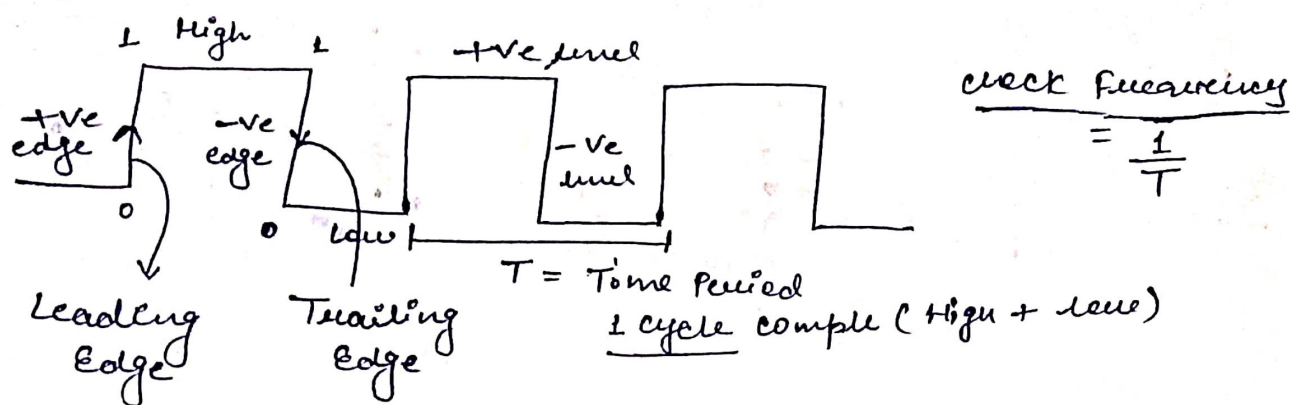
Truth Table SR LATCH USING NAND GATE :-

S	R	Q	$\bar{Q}$
0	0	NOT USED	
0	1	1	0
1	0	0	1
1	1	Previous state	

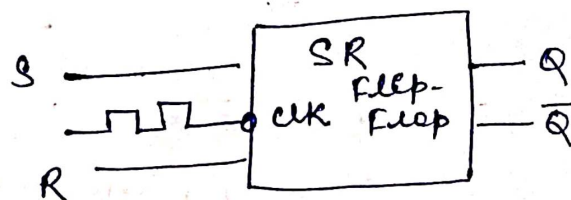
Clock & Triggering Methods

5.

- Clock Signal is a Timing Signal.
- It is used to provide sequence of the ckt.
- clock is a rectangular signal called clock Pulse with duty cycle equal to 50%.



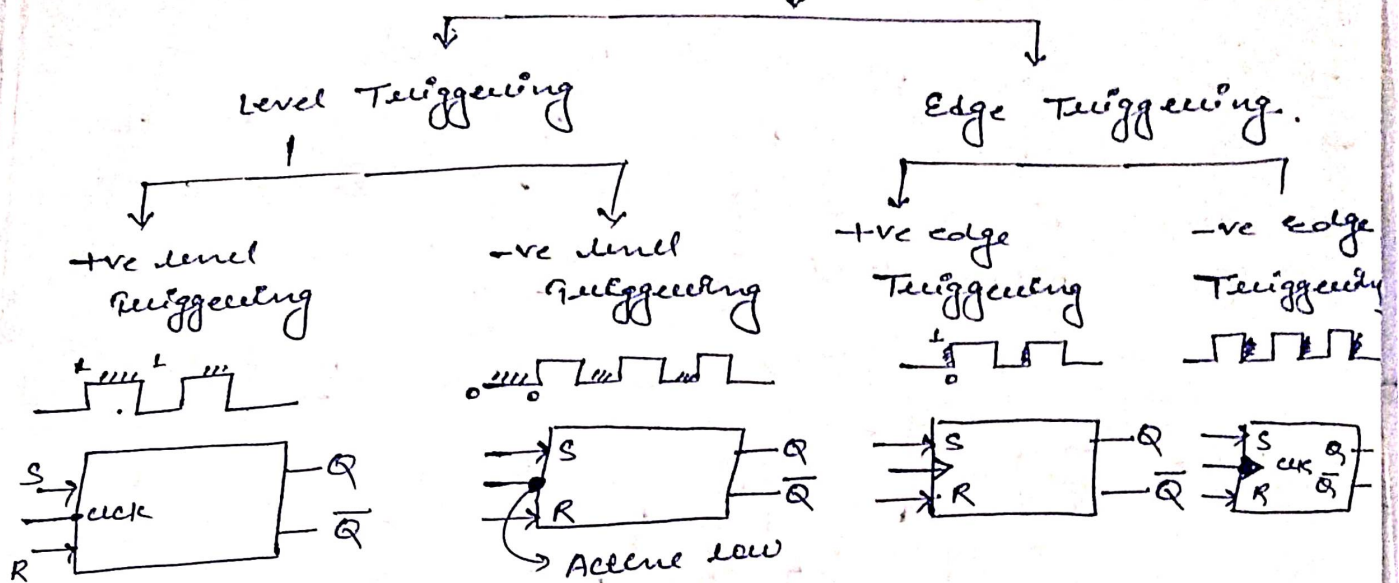
latch behaves like Asynchronous becoz latches change the i/p & it effects the O/Ps.
 if any noise / Hazards are there due to this O/P may vary.



→ Behaves like Synchronous ckt & use like Sequential ckt.

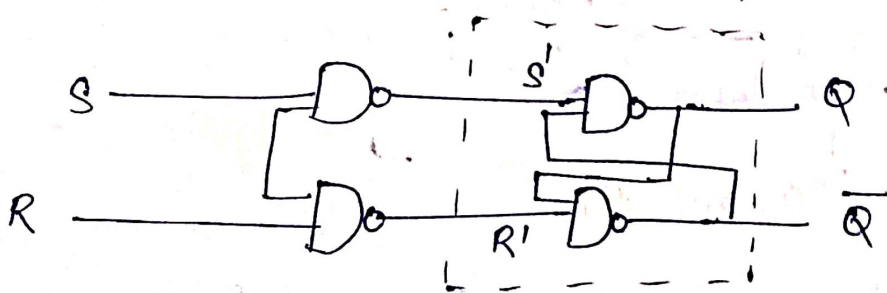
→ when change in the i/p than clk Pulse decide that O/P change or not.

Triggering Methods



SR Flip Flop :- SET RESET FLIP-FLOP

- we are using both latch & flip flop to store one bit of memory element.
- Flip-flop is sequential ckt & use synchronous ext.



Truth Table of SR latch with NAND Gate :-

S'	R'	Q	Q'
0	0	NOT USED	
0	1	1	0
1	0	0	1
1	1	Pre State (Memory)	

$$S' = \overline{S \cdot CLK}$$

$$S' = \overline{S} + \overline{CLK} \quad \text{--- (1)}$$

$$R' = \overline{R \cdot CLK}$$

$$R' = \overline{R} + \overline{CLK} \quad \text{--- (2)}$$

CLK = 0

$$S' = \overline{S} + 1 = 1 \quad \text{0 or 1}$$

$$R' = \overline{R} + 1 = 1 \quad \text{0 or 1}$$

IInd case $clk = 1$

$$S' = S + 0 = S$$

output

$$R' = \bar{R} + 0 = \bar{R}$$

$$1) \left. \begin{array}{l} S' = S \\ R' = \bar{R} \end{array} \right\} \begin{array}{l} 1) S=0, R=0 \\ \quad S'=0, R'=1 \end{array}$$

$$ii) \begin{array}{l} S=0, R=1 \\ S'=1, \bar{R}=0 \end{array}$$

$$iii) \begin{array}{l} S=1, R=0 \\ S'=0, R'=1 \end{array}$$

$$iv) \begin{array}{l} S=1, R=1 \\ S'=0, R'=0 \end{array}$$

clock :- $clk = 0$
 $clk = 1$



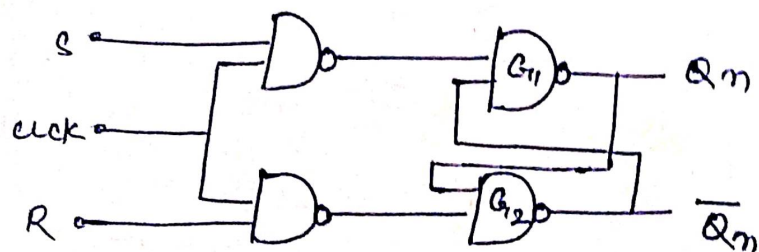
Truth Table of SR FF

clk	S	R	Q	$\bar{Q}$
0	x	x	Pre state	memory.
1	0	0	Pre state	
1	0	1	0	1
1	1	0	1	0
1	1	1	Not Used.	(Invalid O/P)

AND Gate		OR Gate
A	B	$A+B$
0	0	0
0	1	1
1	0	1
1	1	1

Characteristic Equation For SR FF :-

when we convert a FF to another FF then we need to this Equⁿ.



Present state = Q_m

Next State = Q_{m+1}

Truth Table for SR FF

CLK	S	R	Q_{n+1}
0	x	x	Q_n
1	0	0	Q_n
1	0	1	0 Reset
1	1	0	1 Set
1	1	1	Invalid

Characteristic Table :-

Q_n	S_n	R_n	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	(x) don't care (d)
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	d(x) - don't care

$R_n S_n$		00	01	11	10
Q_n	0	0	0	x	1
	1	1	0	x	1

$$Q_{n+1} = R_n + Q_n \bar{S}_n$$

characteristic equation
for SR FF.

Excitation Table For SR FF :-

when we design a counter than we need to this excitation Table For SR FF.

O/P

Present State	Next State	I/P	
Q_n	Q_{n+1}	S_n	R_n
0	0	0	0
0	1	1	0
1	0	0	1
1	1	x	0

char. Table

Q_n	S_n	R_n	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	x
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	x

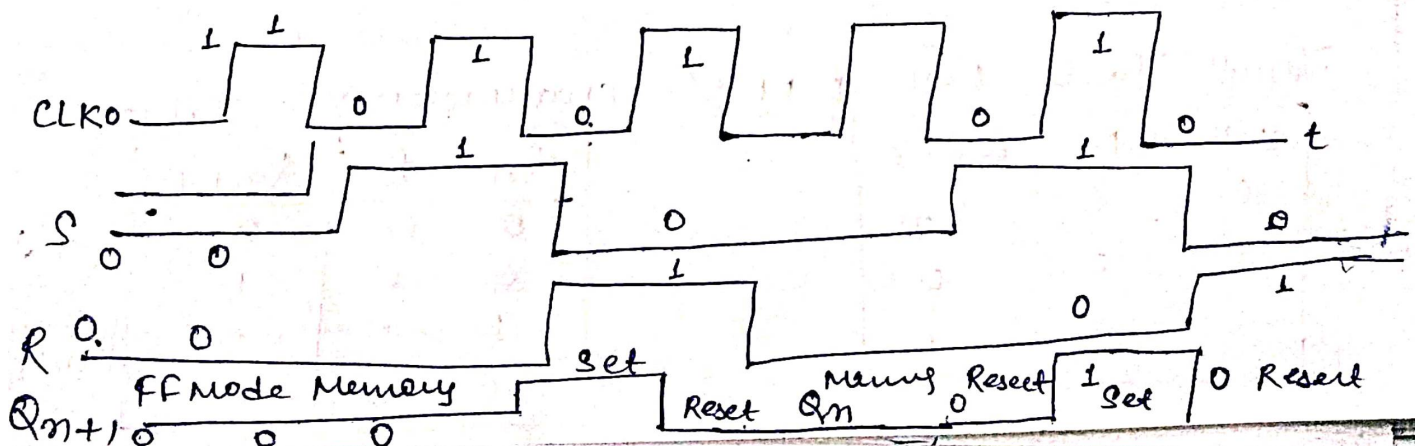
Timing Diagram For SR FF :-

Truth Table For SR FF

CLK	S	R	Q_{n+1}
0	x	x	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	invalid

Truth Table

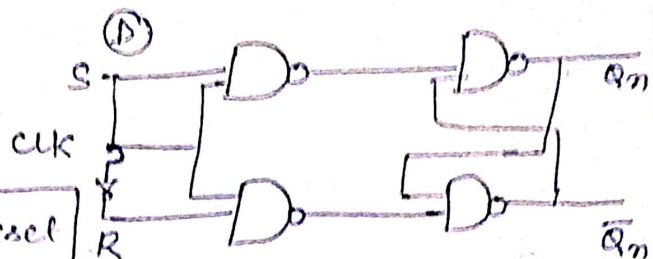
S_n	R_n	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	?



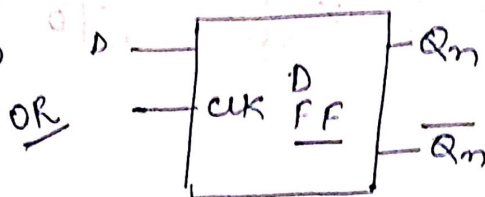
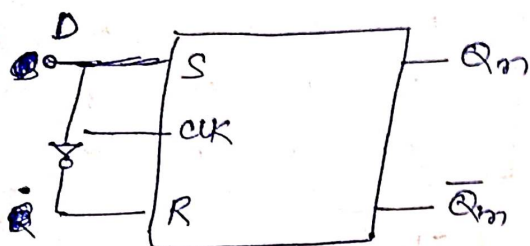
D Flip Flop

Truth Table of SR FF :-

CLK	S	R	Q_{n+1}
0	X	X	Q_n
1	0	0	Q_n
1	0	1	0 $\rightarrow$ Reset
1	1	0	1 $\rightarrow$ Set
1	1	1	Invalid



$S=1, R=0 \quad Q_n=1$ Set
 $S=0, R=1 \quad Q_n=0$ Reset



CLK	D	Q_{n+1}
0	X	Q_n
1	0	0
1	1	1

when clock pulse 0 then it store the data of previous state. (Memory)
 when we change the clock pulse 1 then it change the o/p accordingly.

$\rightarrow$ D flip flop is known as "Data Flip Flop".

Characteristic Equation & Excitation Table for D-FF :-

Truth Table for D FF :-

CLK	D	Q_{n+1}
0	X	Q_n
1	0	0
1	1	1

Characteristic Table

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

$Q_{n+1} = D$

11

	Q_n	0	1
D	0	0	0
	1	1	1

$Q_{n+1} = D$

Excitation Table :- This Table is used for counter to find Present or previous State O/P & find input of the FF

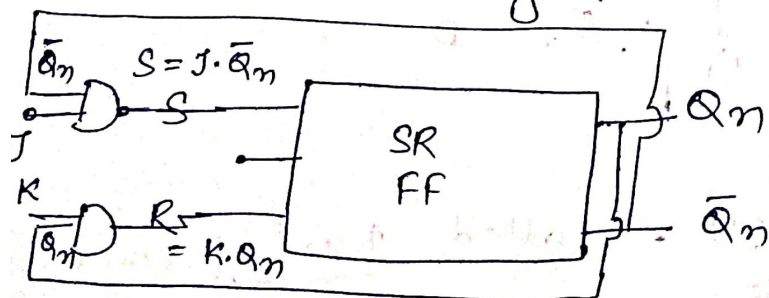
Present State	Next State	O/P
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

	Q_{n+1}	0	1
Q_n	0	0	1
	1	0	1

$Q_{n+1} = D$

JK Flip-Flop

The JK FF is basically a gated SR FF with the addition of a clock input circuitry that prevents the illegal or invalid O/P conditions that can occur when both input S & R are equal to logic level '1'.



CLK	S	R	Q_{n+1}
0	X	X	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	Invalid

12.

J	K	Q_n	$\overline{Q}_n$	$S = \overline{J} \cdot \overline{Q}_n$	$R = K \cdot Q_n$	Q_{n+1}
0	0	0	1	0	0	0
0	0	1	0	0	0	1
0	1	0	1	0	0	0
0	1	1	0	0	1	0
1	0	0	1	1	0	1
1	0	1	0	0	0	1
1	1	0	1	1	0	0
1	1	1	0	0	1	0

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

Assume $Q_n = 0$

1) $Q_n = 1$ 2) $Q_n = 0$

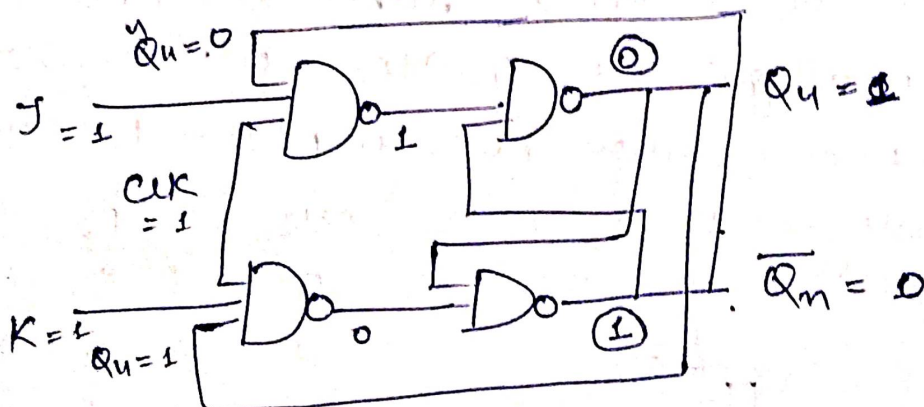
$\overline{Q}_n = 0$ $\overline{Q}_n = 1$

get opposite in both the cases.

& if we feed again then again o/p change $\rightarrow$ Racing b/w 0 & 1, complement of $J = 1$ o/p.

$Q_n = 1$ $K = 1$

wrong.

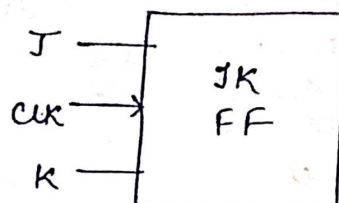


$\overline{Q}_n \rightarrow$ Not predictable $\rightarrow$ called Racing condition

Race Around Condition

Truth Table For JK FF :-

clk	J	K	Q_{n+1}
0	x	x	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	$\bar{Q}_n$



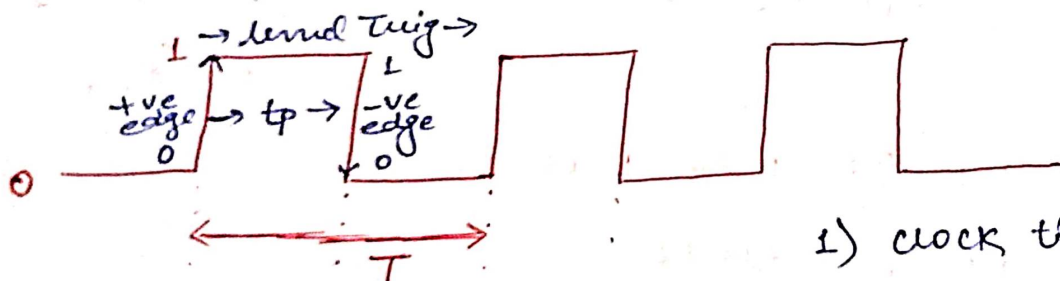
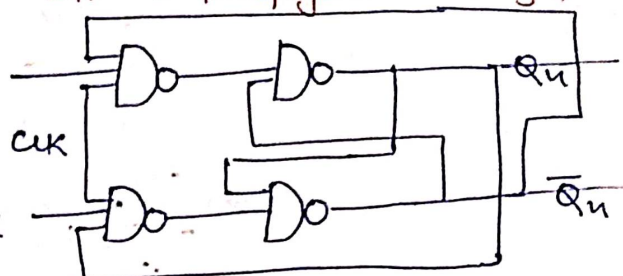
IP $\rightarrow$ Propagation Delay $\rightarrow$ O/P

$clk = 1, J = 1, K = 1$

$\bar{Q}_n = 1, 0, 1, 0, \dots$

$Q_n = 0, 1, 0, 1, \dots$

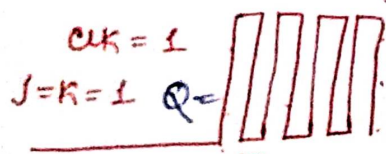
This is called "Racing".



1) clock time

$t_p <$ Propagation Delay

$\rightarrow$ Nanoseconds only



Multiple oscillation

2) Edge Triggering

$\rightarrow$ -ve Edge Trigg.

$\rightarrow$ -ve Edge Trigg.

$\rightarrow$ Master Slave

JK FF

Characteristic Equation 2 Excitation Table For JK FF

14.

Truth Table
For JK FF

clk	J	K	Q_{n+1}
0	X	X	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	$\bar{Q}_n$

Characteristic
Table For
JK FF

Q_n	J	K	Q_{n+1}
0	0	0	$0 = Q_n$
0	0	1	0
0	1	0	1
0	1	1	$\bar{Q}_n = 1$
1	0	0	$Q_n = 1$
1	0	1	0
1	1	0	1
1	1	1	$\bar{Q}_n = 0$

Excitation Table
For JK FF

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

$Q_n \backslash JK$	00	01	11	10
0	0	0	1	1
1	1	0	0	1

$$Q_{n+1} = \bar{Q}_n J + Q_n \bar{K}$$

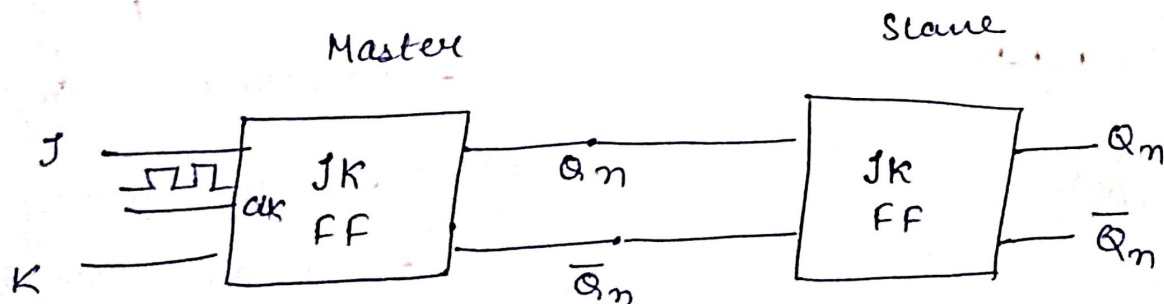
$Q_n \backslash Q_{n+1}$	0	1
0	0	1
1	X	X

$Q_n \backslash Q_{n+1}$	0	1
0	X	X
1	1	0

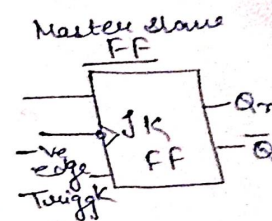
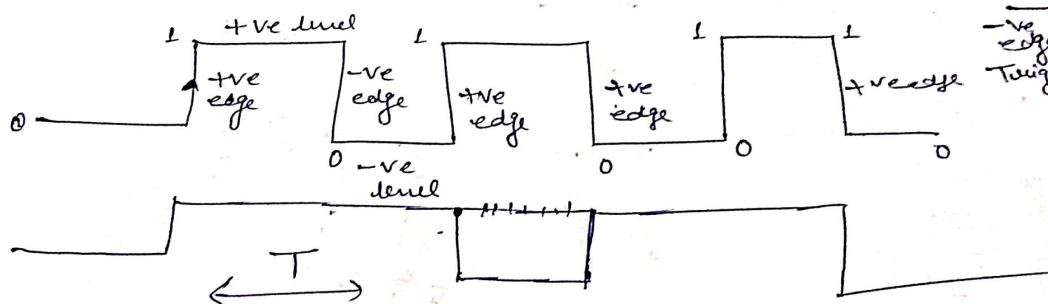
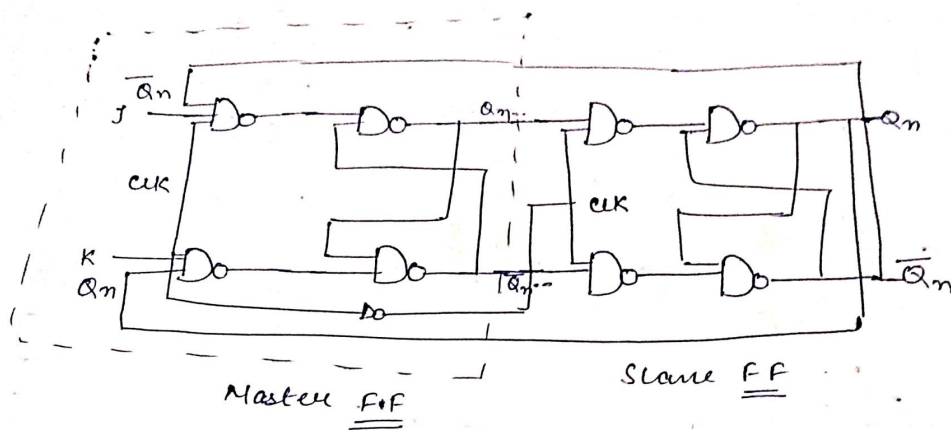
$$K = \bar{Q}_{n+1}$$

Master-Slave JK Flip-Flop

→ One FF is - Master
another is slave.



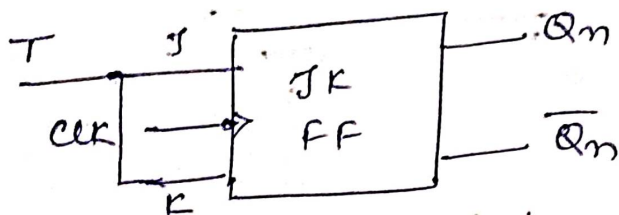
15.



$CLK = 1, J = 1, K = 1, Q_m = \text{Toggle}$

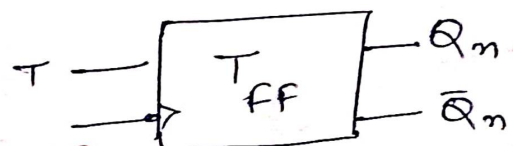
Toggle FF :- T FF $\rightarrow$ This is for toggling the S/P.

$\rightarrow$ we are using JK flip flop for T FF.



clk	J	K	Q_{n+1}
0	X	X	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	$\bar{Q}_n$

clk	T	Q_{n+1}
0	X	Q_n
1	0	$Q_n \rightarrow J=0, K=0$
1	1	$\bar{Q}_n \rightarrow J=1, K=1$



Characteristic Table of T FF :-

Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

$Q_n \backslash T$	0	1
0	0	1
1	1	0

$$Q_{n+1} = Q_n \bar{T} + \bar{Q}_n T$$

$$Q_{n+1} \rightarrow Q_n \oplus T$$

Excitation Table of T FF :-

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

FLIP FLOP CONVERSION

→ JK Flip Flop to T Flip Flop :-

Step-1 Identify available & Required FF
Available → JK FF
Required → T FF

Step-2 Make excitation table for Available FF.

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step-3 Make characteristic table for Required FF

Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Step-4 write Boolean Expression for available FF. 18.

Q_n	T	Q_{n+1}	J	K
0	0	0	0	X
0	1	1	1	X
1	0	1	X	0
1	1	0	X	1

For J =

Q_n	T	0	1
0		0	1
1		X	X

$$J = T$$

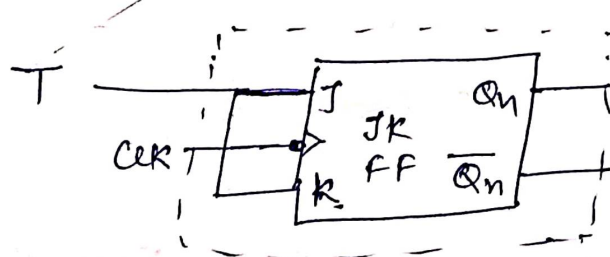
For K =

Q_n	T	0	1
0		X	X
1		0	1

$$K = T$$

$$J = K = T$$

Step-5. Draw the circuit diagram :-



T FF

2. JK FF to D FF :-

19.

- 1) Identify available & Required FF.
- 2) Make available-Excitation table for available FF.
- 3) Make characteristic table for required FF.
- 4) write Boolean Expression for the available FF.
- 5) Draw the CKT diagram.

→ (1) Available - JK
Required - D

→ (2) Excitation Table for JK

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

→ (3) Characteristic Table for D

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

4.

Basically we extend the characteristic 20.
Table for Boolean Expression

Q_n	D	Q_{n+1}	J	K
0	0	0	0	X
0	1	1	1	X
1	0	0	X	1
1	1	1	X	0

For $J =$

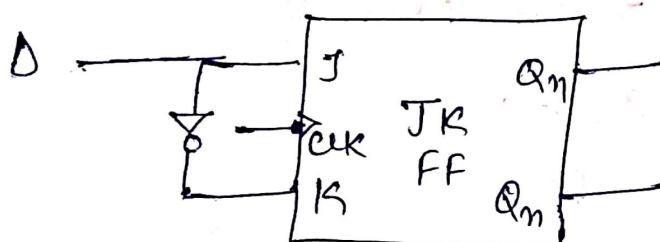
Q_n	D	0	1
0		0	1
1		X	X

$$J = D$$

For $K =$

Q_n	D	0	1
0		X	X
1		1	0

$$K = \overline{D}$$



D Flip Flop

JK FF to SR FF :-

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Step-1 Available FF = JK
Required FF = SR

Step-2 Excitation Table for Available FF.

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step-3 Characteristic Table for Required FF

Q_n	S	R	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	Invalid (X)
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	Invalid (X)

Step-4 Boolean Expression for Available FF.

Q_n	S	R	Q_{n+1}	J	K
0	0	0	0	0	X
0	0	1	0	0	X
0	1	0	1	1	X
0	1	1	Invalid (X)		
1	0	0	1	X	0
1	0	1	0	X	1
1	1	0	1	X	0
1	1	1	Invalid (X)		

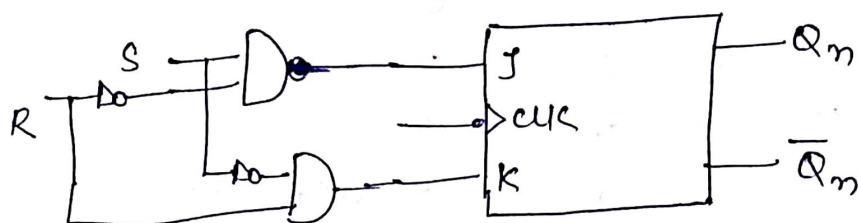
	SR		00	01	11	10
Q_n	0	1	0	0		1
	1	0	1	1		0

$$Q_{n+1} = J = S\bar{R}$$

	SR		00	01	11	10
Q_n	0	1	1	0		1
	1	0	0	1		0

$$K = \bar{S}R$$

Step-5 Draw the circuit diagram :-



JK to SR Flip-Flop

SR FF to JK FF :-

- 1) Available = SR
Required = JK

2) Excitation Table $\rightarrow$ SR

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

3) Characteristic table for $\rightarrow$ JK

Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

4) Boolean Expression for SR.

Q_n	J	K	Q_{n+1}	S	R
0	0	0	0	0	X
0	0	1	0	0	X
0	1	0	1	1	0
0	1	1	1	1	0
1	0	0	1	X	0
1	0	1	0	0	1
1	1	0	1	X	0
1	1	1	0	0	1

24.

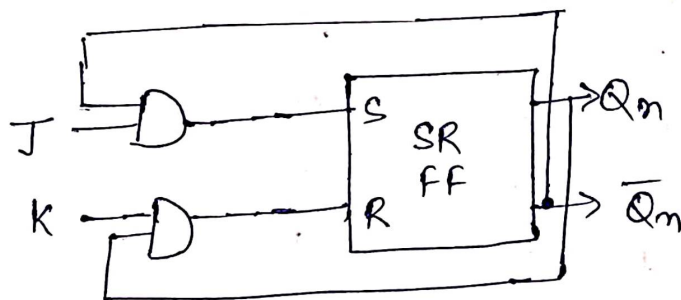
$Q_n \backslash JK$	00	01	11	10
0	0	0	1	1
1	X	0	0	X

For $S = \overline{Q_n} J$

$Q_n \backslash JK$	00	01	11	10
0	X	X	0	0
1	0	1	1	0

For $R = Q_n K$

Step-5 Draw the circuit Diagram for this:-



SR to JK flip flop

SR FF To T FF :-

Step-1 = Available FF $\rightarrow$ SR
Required FF $\rightarrow$ T

Step-2 = Excitation Table $\rightarrow$ SR

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Step-3 = Characteristic table for T

Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Step-4 = Boolean Expression for SR

Q_n	T	Q_{n+1}	S	R
0	0	0	0	X
0	1	1	1	0
1	0	1	0	1
1	1	0	X	0

$Q_n \backslash T$	0	1
0	0	1
1	0	X

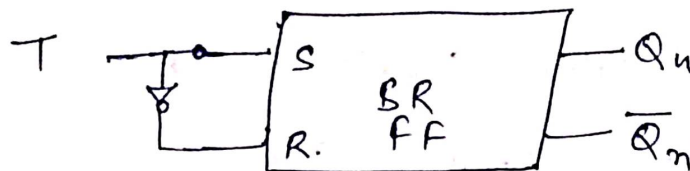
$$S = T$$

$Q_n \backslash T$	0	1
0	X	0
1	1	0

$$R = \overline{T}$$

26.

Step - 5 :- Draw the circuit Diagram for this.



SR FF To T FF

SR to D FF :-

1) Available - SR
Required $\rightarrow D$

2) Excitation $\rightarrow SR$

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

3) Characteristic - D

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

27.

Boolean Expression for SR :-

Q_n	T	Q_{n+1}	S	R
0	0	0	0	X
0	1	1	1	0
1	0	1	0	1
1	1	0	X	0

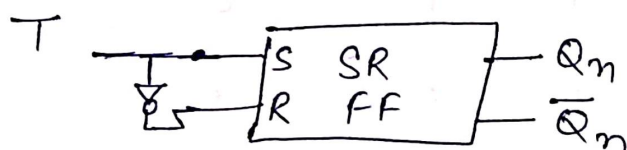
Q_n	T	Q_{n+1}
0	0	1
0	1	1
1	0	X

$S = T$

Q_n	T	Q_{n+1}
0	0	1
0	1	X
1	1	0

$R = \overline{T}$

Q. Draw the circuit diagram for this :-



SR FF To T FF

SR to JK FF :-

1) Available $\rightarrow$ SR
Required $\rightarrow$ JK

2) Excitation Table $\rightarrow$ SR

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

3.) characteristic $\rightarrow$ JK

Q_n	Q_{n+1}	J	K	Q_{n+1}
0	0	0	0	0
0	1	0	1	0
0	0	1	0	1
0	1	1	1	1
1	0	0	0	1
1	1	0	1	0
1	0	1	0	1
1	1	1	1	0

4) Boolean Expression for SR -

Q_n	J	K	Q_{n+1}	S	R
0	0	0	0	0	X
0	0	1	0	0	X
0	1	0	1	1	0
0	1	1	1	1	0
1	0	0	1	0	0
1	0	1	0	0	1
1	1	0	1	0	0
1	1	1	0	0	1

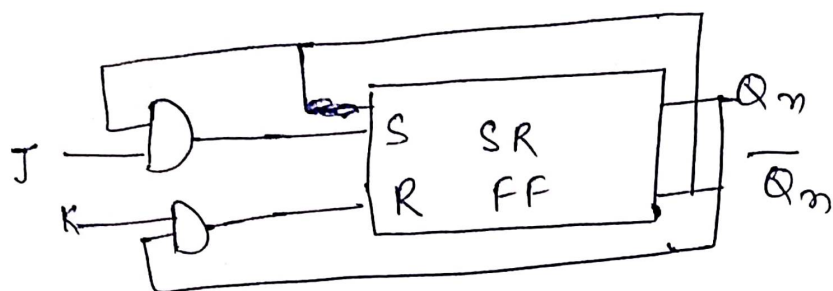
29.

	00	01	11	10
Q_n	0	0	1	1
J	X	0	0	X

$$S = \bar{Q}_n J$$

	00	01	11	10
Q_n	X	X	0	0
K	0	1	1	0

$$R = Q_n K$$



SR to JK FF