UNIT-3rd Digital logic Gate Characteristic

Basic Needs

Semiconductor devices :- 2 types → Bipolar
→ Unipolar

Bipolar → Both types of charge carrier
↑
Electrons Holes

Unipolar → Only one type of charge carriers :-
i.e flow the current.

we use here switching property of this :-

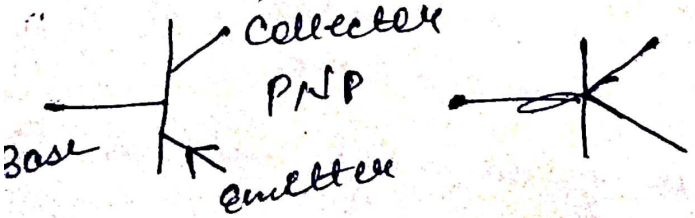
Diode → PN Junction Diode

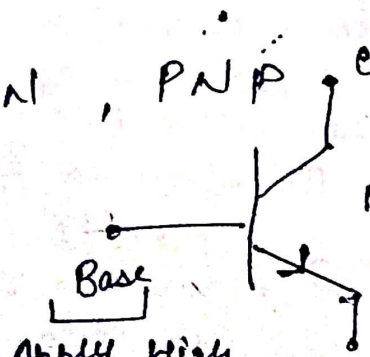
→ unidirectional property follow

F.B → P → Anode → +Ve Terminal of Battery
→ N → Cathode → -Ve Terminal of Battery
→ So it work as ON switch

R.B → OFF Switch.

Transistor :- NPN , PNP





Low-Base Voltage
↳ off Switch

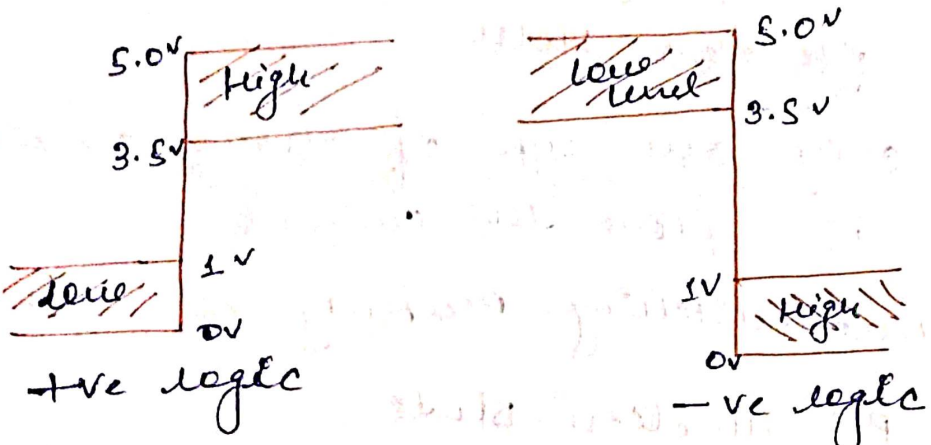
Logic Family :- A group of compatible ICs with same logic level and supply voltage fabricated for performing various logic functions referred as a logic family.

→ OR, NOT, AND, etc.

IC → Integrated circuit → chip

↓

1000 of Transistor fabricated of that chip.



These level are different for different logic family.

Digital IC

- Bipolar logic family
  - → (use both electrons & holes as a charge carries)
  - ↳ register, Transistor, Diode are mainly used in Bipolar logic family.
  - Saturated
    - ↳ 1) RTL, 2) DTL, 3) DCTL, 4) TTL
  - Non-saturated
    - ↳ 5) IIL, 6) HTL, ECL,
- Unipolar logic family
  - → (use only one type of charge carries i.e. Holes or E.)
  - ↳ MOS devices
    - 1) PMOS - P-channel MOSFET
    - 2) NMOS → N-channel MOSFET
    - 3) CMOS - C-channel MOSFET
  - → only work in Active or cut-off Region
- Bi-cmos logic family
  - → I/P → logic OP CMOS
  - → O/P → Bipolar

CMOS :- (Complimenty Metal Oxide Semiconductor field effect Transistor)

Characteristics of Digital ICs :-

1) Propagation Delay, Speed
2) Power Dissipation
3) Figure of Merit
4) Fan-out, Fan-in
5) Noise Immunity, Noise-Margin
6) Operating Temp.
7) current and voltage Parameter.
8) Breadth, logic Swing

Propagation Delay :-

* Propagation Delay is always measured by nano seconds, → 10^{-9} of a secons

If TTL IC :- $t_{PHL} = 7ns$

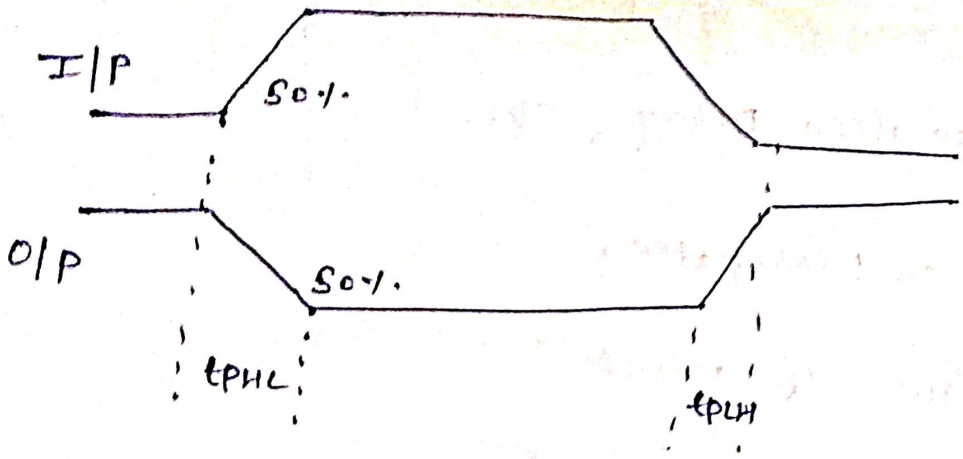
$t_{PLH} = 11ns$

Avg Prog Delay = ?

$= \frac{11+7}{2} = 9ns$

→ Speed of operations is specified in terms of Propagation delay

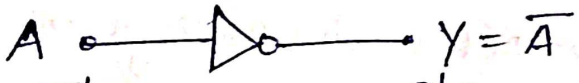
→ Delay Time is measured blw 50% of IP & O/P Transaction.



Avg. Propagation Delay = $\frac{t_{PHL} + t_{PLH}}{2}$

tPHL :- Delay time when O/P goes from High to low

tPLH :- Delay time when O/P goes from low to high



→ Take some time → i.e → Delay

Power Dissipation :-

→ This is the amount of Power dissipation is an IC in the form of Heat.

→ Excessive temp. could damage the IC. so power Dissipation should be le

→ P.D is determined by the current Icc that is drawn from Vcc

P.D = Icc X Vcc

Figure of Merit :-

It is always define as a product of Speed & Power.

Figure of Merit = Propagation delay x Power

→ ns x mw

→ 10^{-9} sec x 10^{-3} W

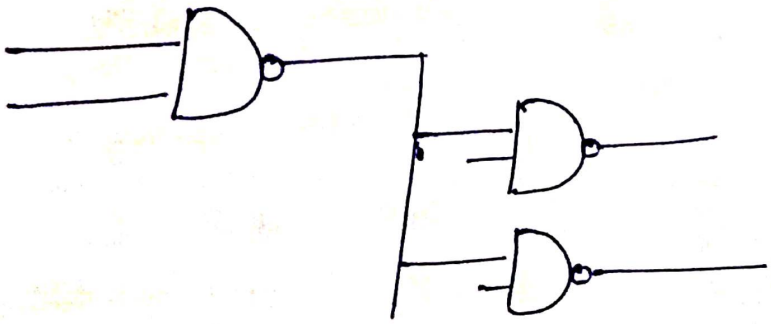
→ 10^{-12} Joules or Pico Jules

⇒ 10^{-12} PJ

Fan-Out :-

No. of similar gates which can be driven by a Gate.

→ Higher the fan-out, higher the current supplying capacity of a gate.



To other I/Ps

Voltage Parameter :-

- I_{IL}, I_{OL} — Current flow
- V_{IL}, V_{OL} — Current flow

Current flow:
- Low level I/P
- High level I/P
- Low level O/P
- High level O/P

} Voltage

Noise Margin :- It is the limit of Noise Margin that can be present without disturbing proper operation of the circuit.

The circuit ability to tolerate Noise Signal is referred to Noise immunity.

Operating Temp. :- at which Temp IC's operates.

0 to 70°c → Commercial Purpose

-55°c to 125°c → Military Application

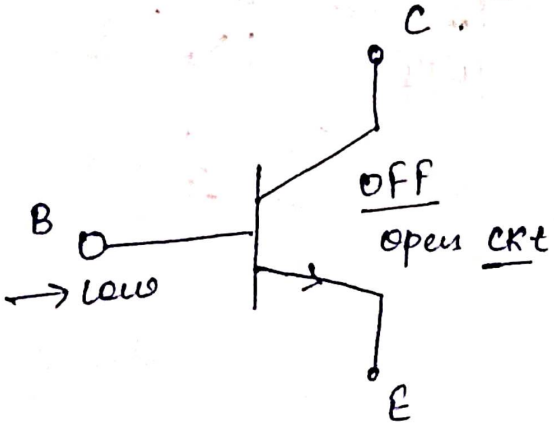
RTL

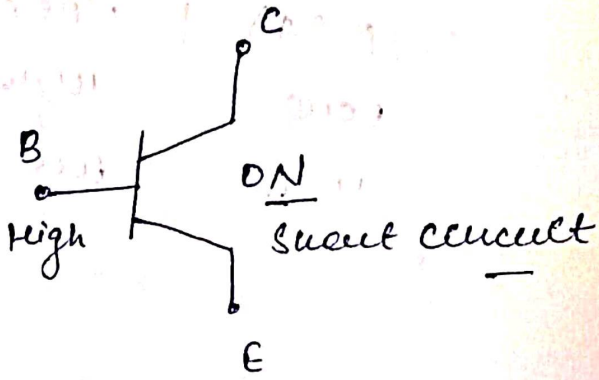
Register Transistor logic

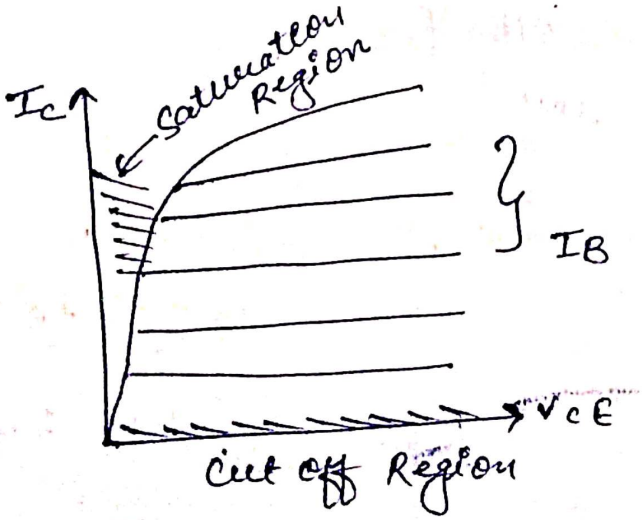
In this we use Register & Transistor to design RTL logic. OR we use here NOR Gate.
↳ universal gate

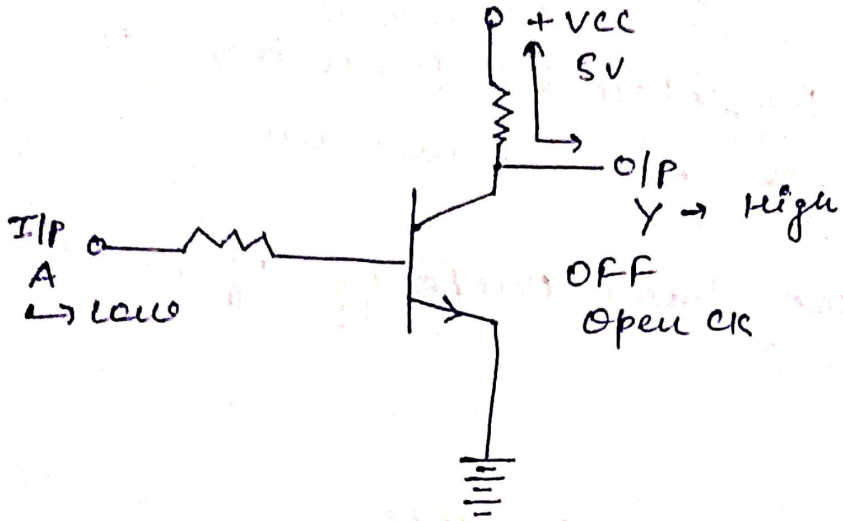
In this we use basic property of transistor
i.e → ON
→ OFF

→ Cut-Off Region → Off State → Open circuit
→ Saturation Region → ON State – S.C

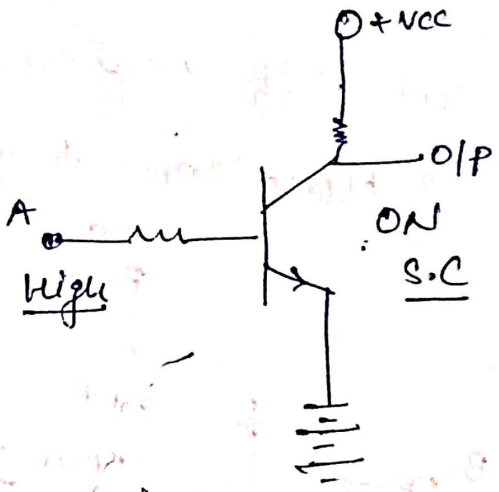


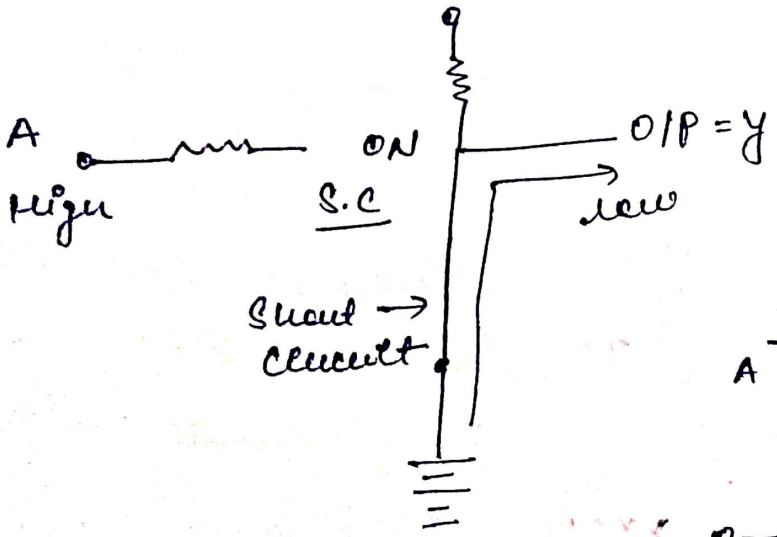


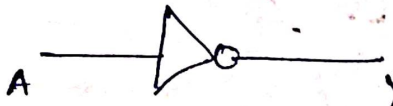




I/P (A)	O/P (Y)
Low	High
High	Low







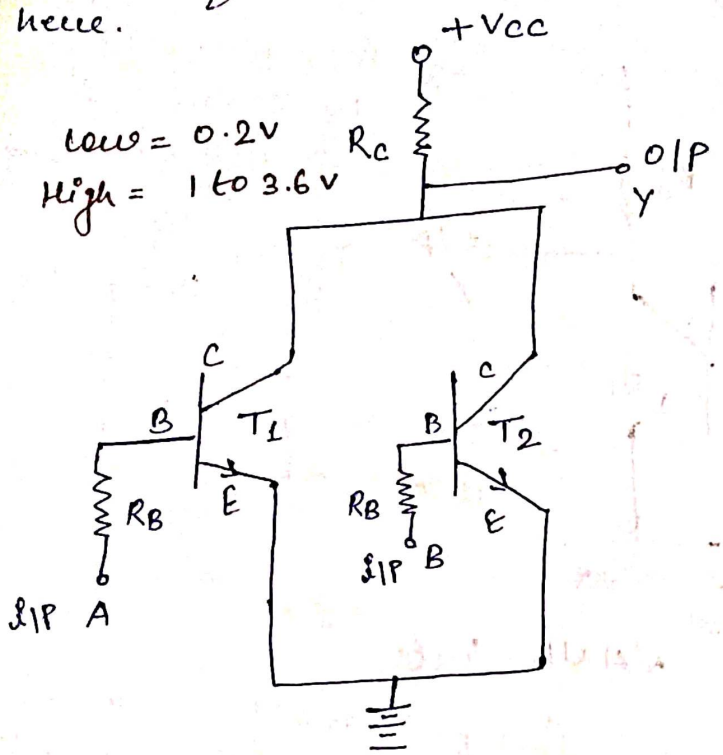
NOT Gate

RTL Inverter Logic

Register Transistor logic

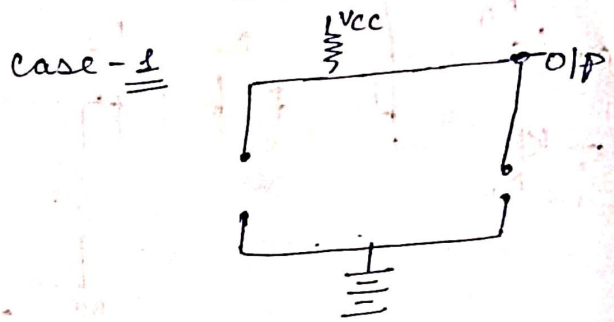
We use here n no. of I/P here.

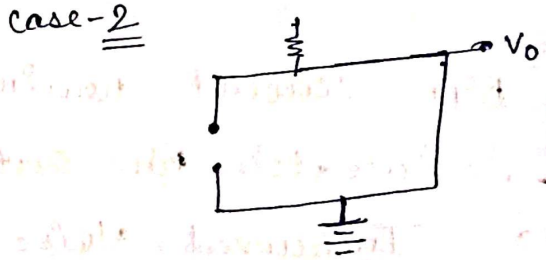
Basic gate - NOR



→ Base is connected to I/P

→ Collector is connect with → Vcc





	A	B	Y
1)	Low	Low	High
	Low	High	Low
	High	Low	Low
	High	High	Low

} NOR

Diode Transistor logic (DTL)

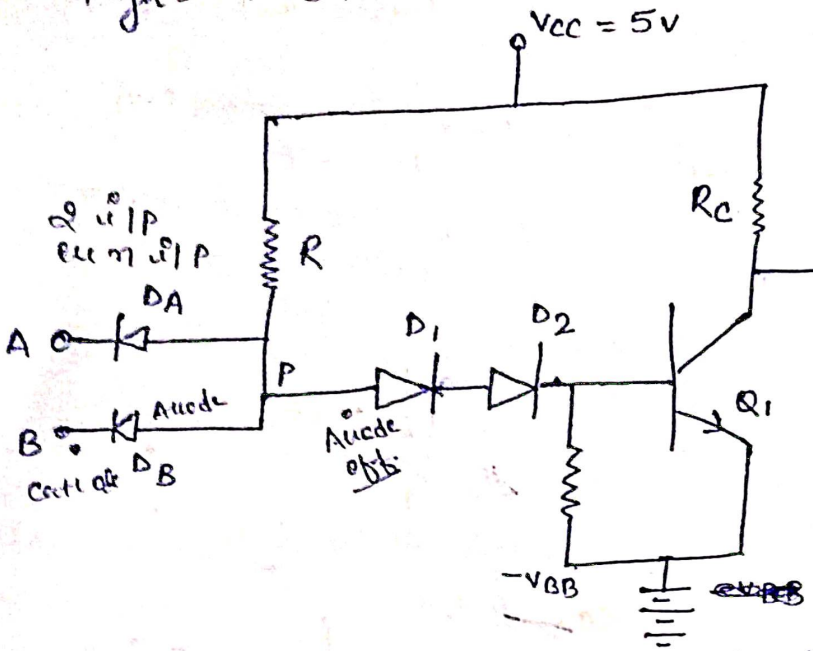
This is upgrade version of RTL in this we improve different characteristic of logic family. i.e. Fan out, Power dissipation, Noise Margin etc.

Power dissipation ↓ very high

Noise Margin → low

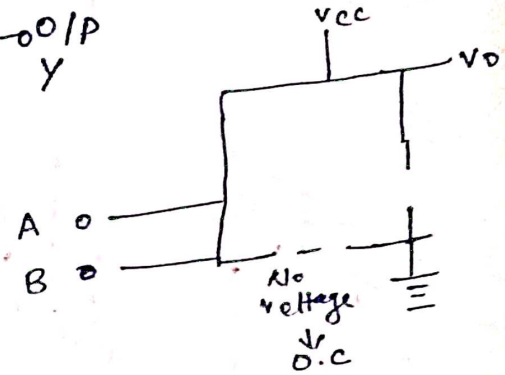
→ We can design NAND Gate here with Transistor & Diode.

Low = 0.2V
High = 4-5V



Basic Gate → NAND

→ Anode must be connected to higher voltage



→ DTL circuit having NAND Gate.

→ Greater fan out

→ Improved Noise Margin

* if Transistor Base is connect with -ve voltage means cut-off → OFFstate → O.C

* Diode → ON → Forward bias → current flow → S.C
OFF - Reverse bias → No current flow → O.C

Transistor → Base → low i/p → OFF → O.C
Base → High i/p → ON → S.C

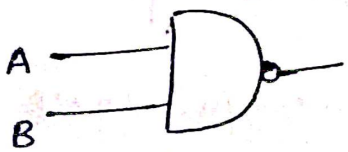
V_{CE} = saturation
low = 0.2V

A	B	Y
0	0	High (1)
0	1	High (1)
1	0	High (1)
1	1	low (0)

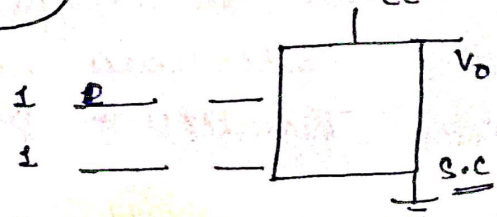
Because of complex circuit

→ Speed slow, Power Dissipation

→ High Fan-out, Noise Margin → TTL Next



4)



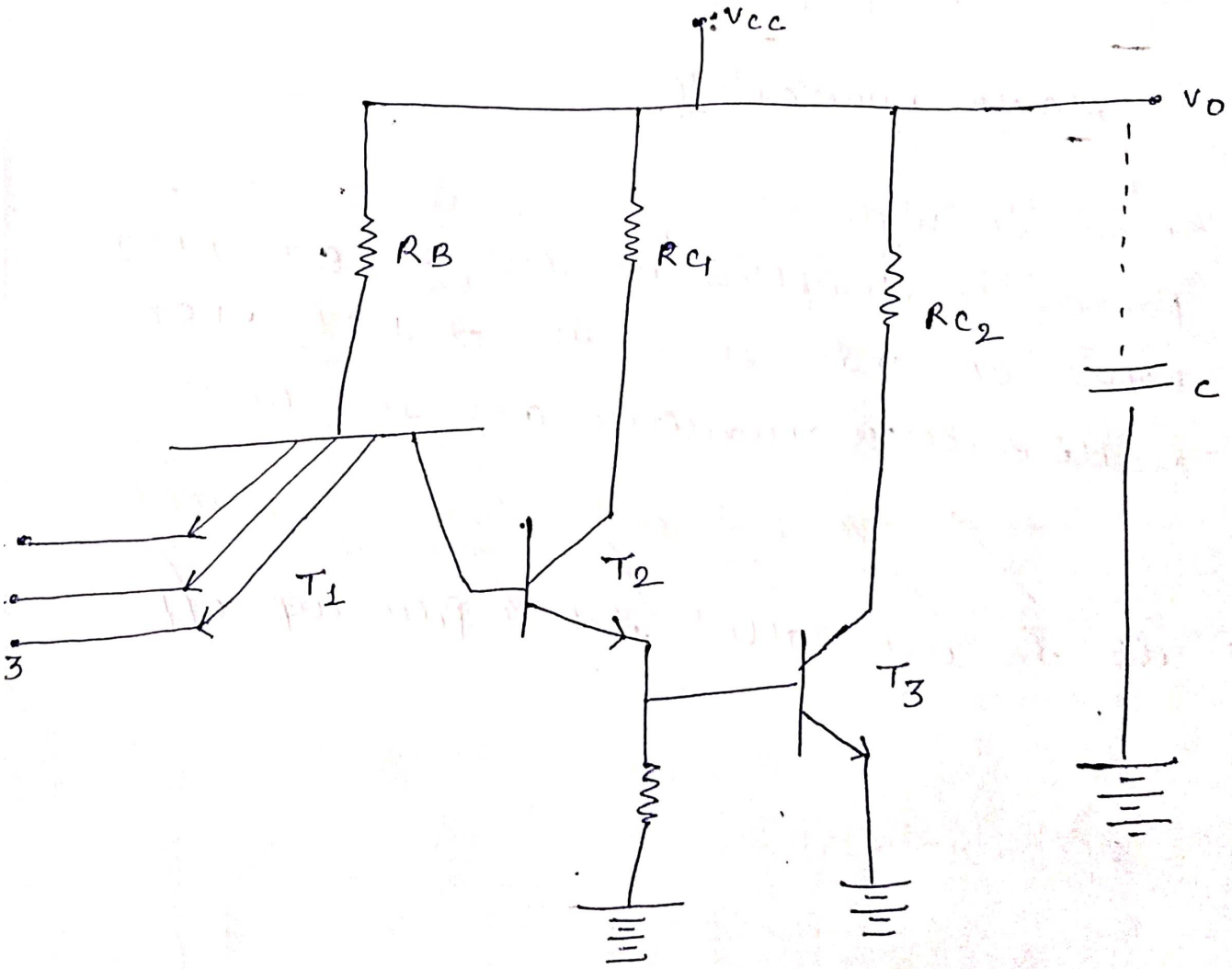
Transistor Transistor Logic

TTL

→ This is just modified circuit of DDL.

→ Here we are using few i/p is multi-emitter Transistor.

→ In this we remove the Diode - D_1 & D_2 with the help of Transistor.



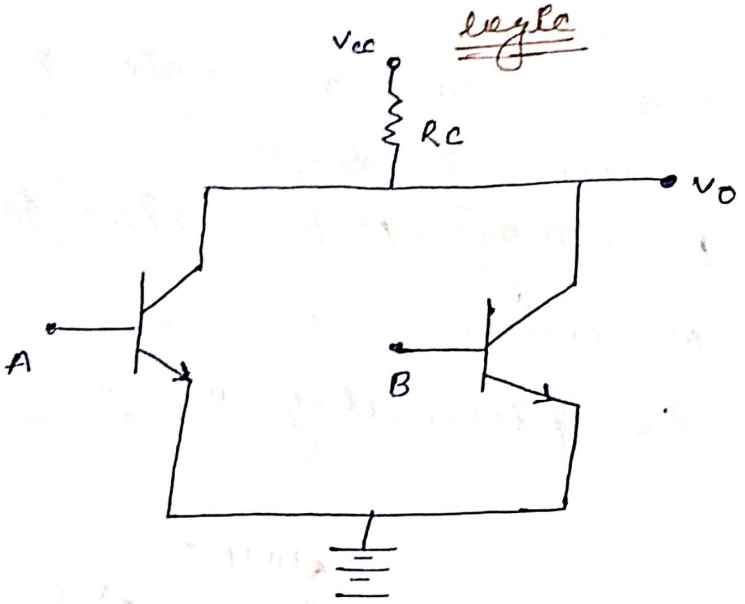
Truth Table :-

A	B	C	V_o
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

NAND Functionality

→ Speed is high
→ Power Consumption is less - SSI, MSI
→ PMOS, CMOS is used in → LSI, VLSI
→ Multi emitter Transistor are use here.

Direct coupled Transistor logic



Basic gate - NOR

In RTL :-

→ Poor Noise Margin

→ More Power Consumption

→ In this I/P directly connected to base of Transistor without using any Register in between Input & Transistor Base

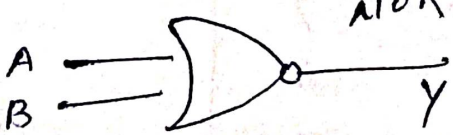
→ functionality is similar to RTL, so here we use NOR Gate.

→ The I/P of Transistor are low, then transistor in cut-off Region → O.C → Path is going to cut

→ The I/P of Transistor are high, the Transistor in Saturated Region → S.C

I/P A	I/P B	O/P V_o
0	0	1
0	1 → ON	0
1	0	0
1	1	0

Off →



we use more N no. of I/P. so we make N no. of NOR Gate

PMOS & NMOS Inverters

→ In this we use unipolar logic family.

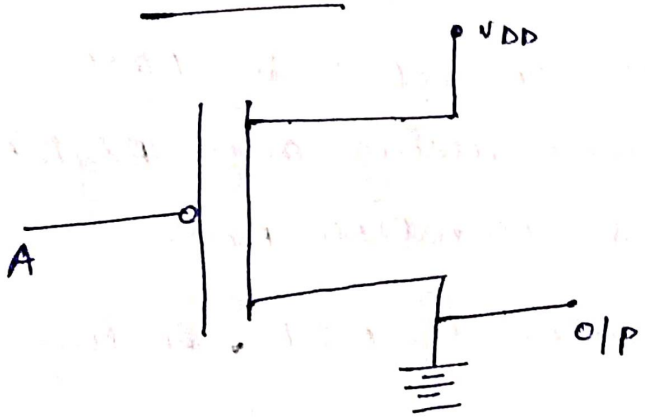
→ current direction is single.

PMOS → P-channel Metal oxide Semiconductor.

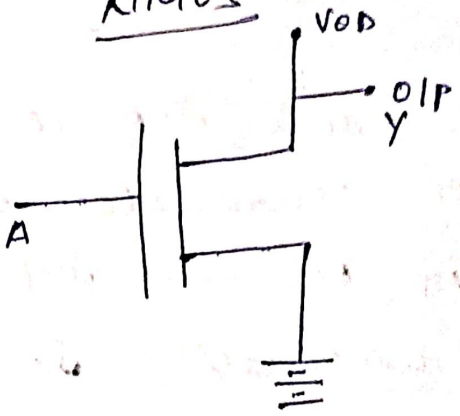
NMOS → N- channel " " "

CMOS → complementary " " "

PMOS



NMOS



Voltage :- PMOS NMOS

0V (0) ON OFF

5V (1) OFF ON

I/P	O/P
A	Y
S.C 0	1
O.C → 1	0

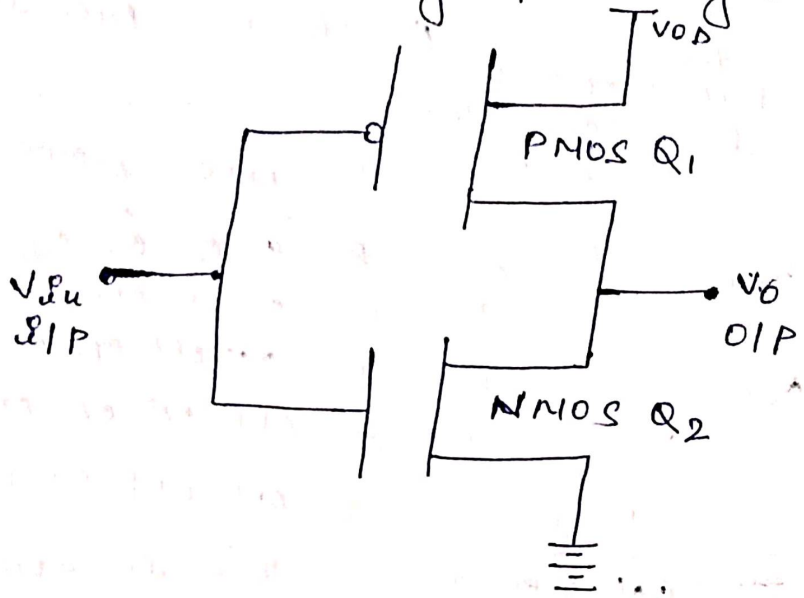
ON
OFF

I/P	O/P
A	Y
O.C → 0	1
S.C → 1	0

OFF
ON

CMOS Inverter

→ It is combination of PMOS & NMOS.
→ It is very fast logic family.



CMOS or CMOS inverter is same & PMOS & NMOS or these inverter is same.

→ NMOS is going to ON for high voltage
→ PMOS is going to ON for low voltage

→

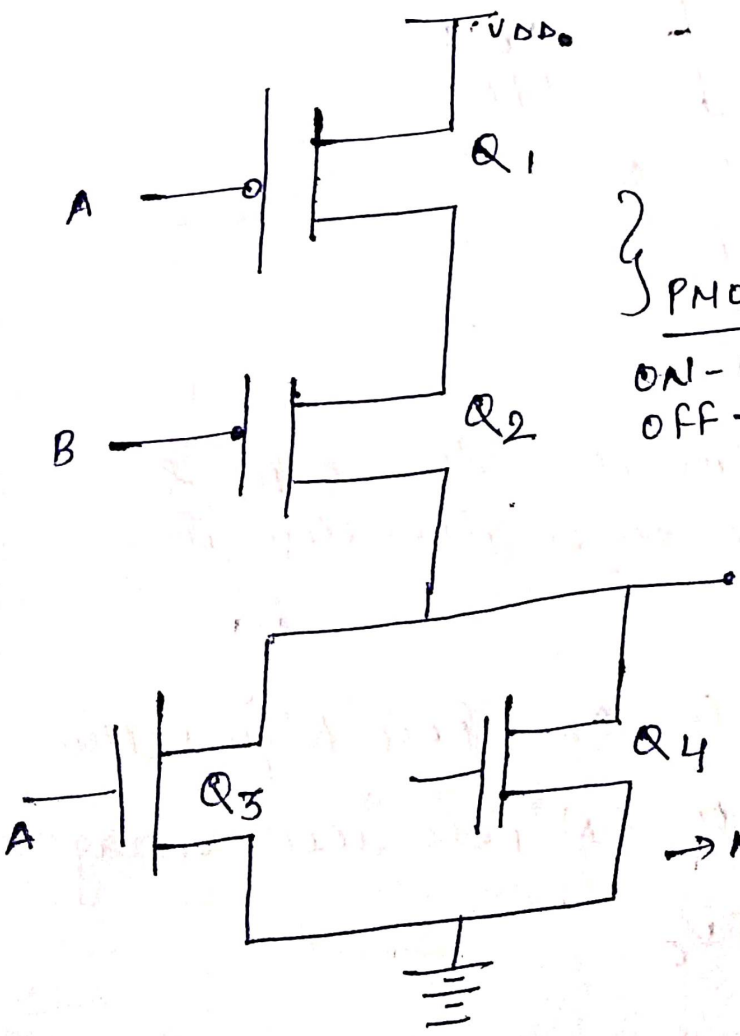
VIN	Q1	Q2	VO
0	ON	OFF	1
1	OFF	ON	0

→ Thats why CMOS also called CMOS Inverter.
→ MSI, Highest speed logic family as compare to other family.

CMOS NOR Gate

→ CMOS NOR Gate use NMOS & PMOS
↓ ↓
use this → Pull down Pull up

use this Functionality for CMOS NOR Gate



PMOS
ON - 0 → S.C
OFF - 1 → O.C

A	B	PMOS Q1	PMOS Q2	NMOS Q3	NMOS Q4	VO
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	0
1	0	OFF	ON	ON	OFF	0
1	1	OFF	OFF	ON	ON	0

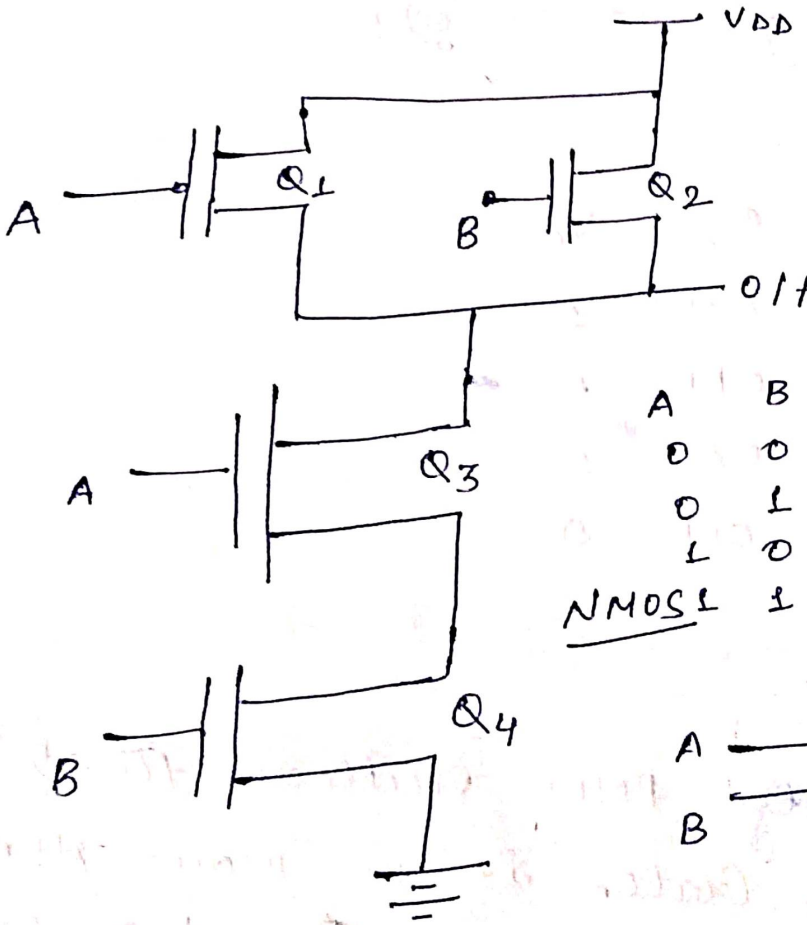
ON - 1 → S.C
OFF - 0 → O.C

This is work as NOR Gate Operation.

CMOS NAND Gate

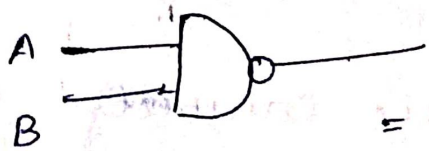
→ CMOS NAND Gate are designed by NMOS & PMOS logic family.

→ In this NMOS is pull up mode & PMOS in pull down mode only.



		P		N		
A	B	Q_1	Q_2	Q_3	Q_4	V_O
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	1
1	0	OFF	ON	ON	OFF	1
1	1	OFF	OFF	ON	ON	0

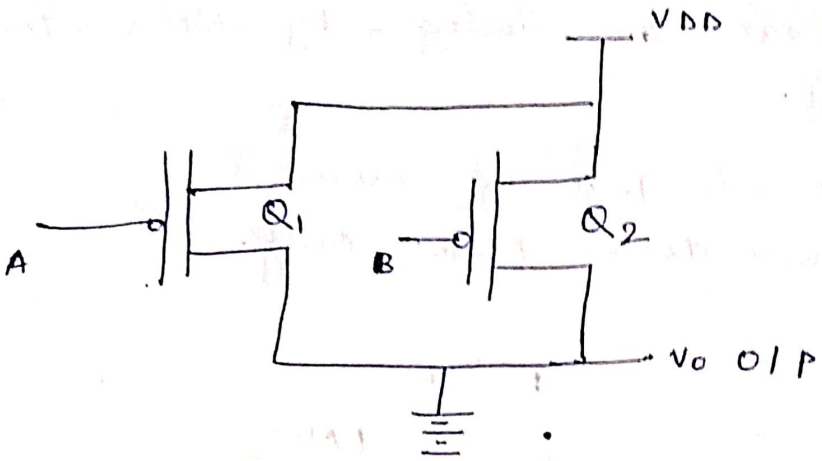
NMOS



NAND Gate

$= \overline{A \cdot B}$

PMOS NAND Gate

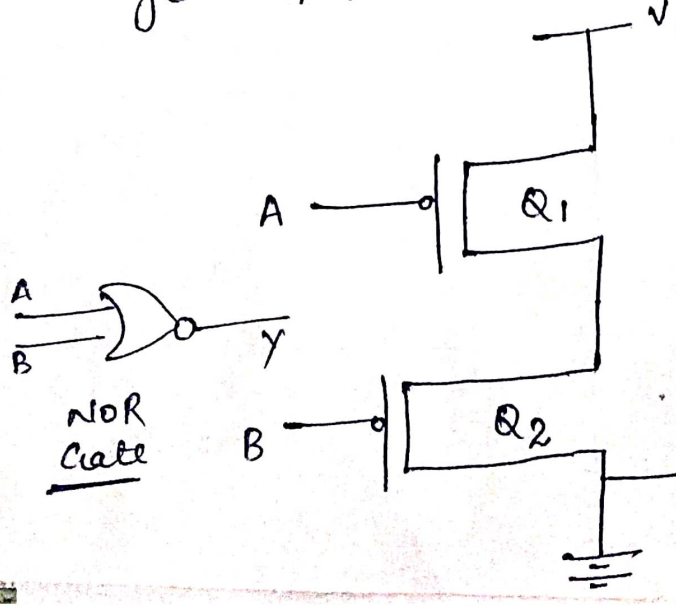


0 – ON – S.C
OFF → 1 – O.C →

A	B	Q_1	Q_2	V_o
0	0	ON	ON	1
0	1	ON	OFF	1
1	0	OFF	ON	1
1	1	OFF	OFF	0

PMOS NOR Gate :

when we connected PMOS vertical than we get PMOS NOR Gate. if we want N no. of O/P than we add no. of I/P here like vertical.



NOR Gate

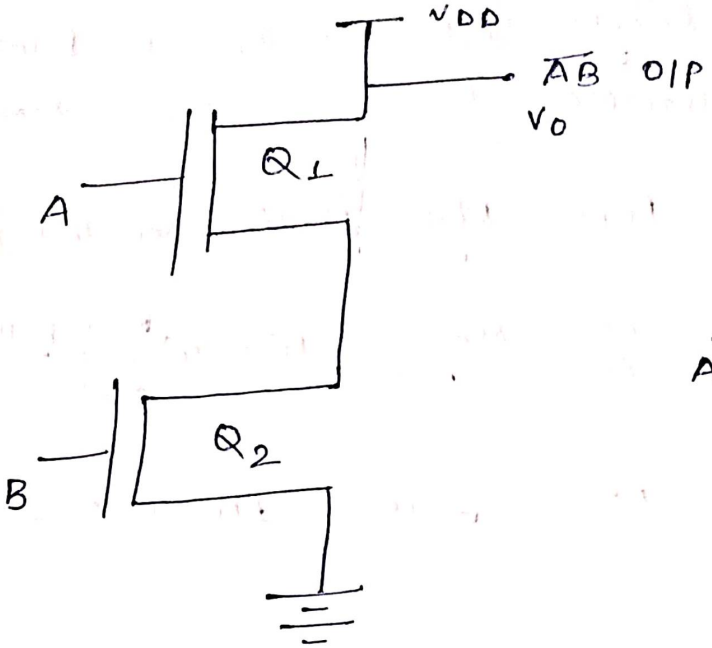
S.C – ON →

OFF → 1

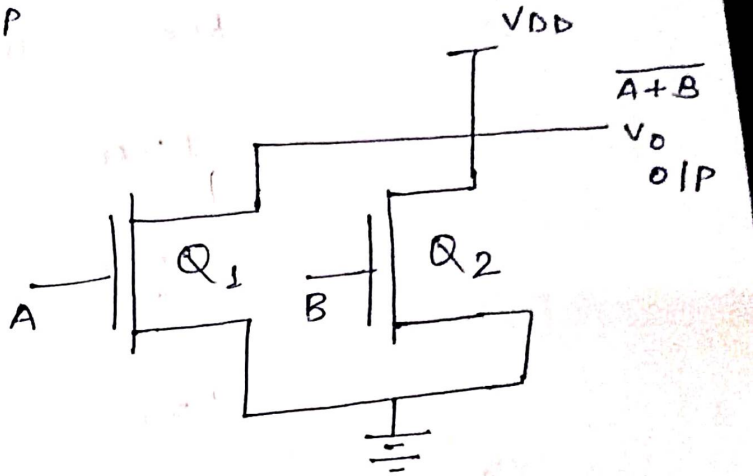
O/P Vr O.C

A	B	Q_1	Q_2	V_o
0	0	ON	ON	1
0	1	ON	OFF	0
1	0	OFF	ON	0
1	1	OFF	OFF	0

Designing Universal Gates using NMOS



NAND



NOR

A	B	Q_1	Q_2	V_O O/P
OFF → 0	0	OFF	OFF	1
↓				
S.C 0	1	OFF	ON	1
1	0	ON	OFF	1
ON → 1	1	ON	ON	0
↑				
S.C				

A	B	Q_1	Q_2	V_O O/P
0	0	OFF	OFF	1
0	1	OFF	ON	0
1	0	ON	OFF	0
1	1	ON	ON	0
		↓		
		S.C		

Comparison of logic family

Parameter	RTL	DCTL	DTL	TTL	ECL	I^2L	CMOS
	Register & Transistor	Register & Transistor	R,D, R,T	R,T	T	T	PMOS NMOS
Components	~~Poor~~						
Noise - Margin	~~Poor~~	Poor	high	Medium	low	high	high
Fan - out	low (4)	low (4)	Medium (8)	high (10)	very high (25)	8-11	50
Power - dissipation (mw)	30	10	8-12	10	40-55	5-25	
Delay (ns)	12	10	30	10	2 (10k) 0.75 (100k)	25-25	
Figure of Merits	144	1300	300	100	100 [10k] 40 [100k]	4	0.7

CMOS → its low power consumption.

ECL its fastest logic family